

What is claimed is:

1. A semiconductor integrated circuit device comprising:  
a logic circuit; and  
a memory cell array on which memory cells are integrated;  
5 wherein the logic circuit has;

a first logic gate including an NMOS transistor having a first threshold voltage and a PMOS transistor having a third threshold voltage; and

10 a second logic gate including an NMOS transistor having a second threshold voltage and a PMOS transistor having a fourth threshold voltage,

the memory cell array is a memory cell array on which a static memory cell comprising two load MOS transistors, two drive MOS transistors, and two transfer MOS transistors is  
15 integrated,

the two load MOS transistors are PMOS transistors each having the fourth threshold voltage,

the two drive MOS transistors are NMOS transistors each having the second threshold voltage,

20 the first threshold voltage is smaller than the second threshold voltage, and

the absolute value of the third threshold voltage is smaller than the absolute value of the fourth threshold voltage.

25 2. A semiconductor integrated circuit device according to

claim 1, wherein the two transfer MOS transistors are NMOS transistors each having the first threshold voltage.

3. A semiconductor integrated circuit device according to  
5 claim 1 or 2,

wherein the memory cell array is formed by a plurality of banks,

the memory cell and a pair of bit lines are connected in each of the banks, and

10 the pair of bit lines in each of the banks are connected to a pair of global bit lines which extend in the plurality of banks via a switch MOS device.

4. A semiconductor integrated circuit device according to any  
15 one of claims 1 to 3, wherein a gate oxide film in each of the NMOS and PMOS transistors in the logic circuit and the memory cell array has a first thickness.

5. A semiconductor integrated circuit device according to any  
20 one of claims 1 to 4, wherein a difference between the first and second threshold voltages is according to a dose of a first impurity existing in a channel of a transistor, and a difference between the third and fourth threshold voltages is according to a dose of a second impurity existing in a channel of a  
25 transistor.

6. A semiconductor integrated circuit device according to any one of claims 1 to 4, wherein each of a difference between the first and second threshold voltages and a difference between the third and fourth threshold voltages is according to a channel length of each of the transistors.

7. A semiconductor integrated circuit device according to claim 1, wherein the two transfer MOS transistors are NMOS transistors each of which has the same dose of impurity in a channel as that of an NMOS transistor having the second threshold voltage and has a long channel.

8. A semiconductor integrated circuit device comprising:  
a logic circuit; and  
a data input output circuit,  
wherein the circuits include:

an NMOS transistor having a gate oxide film of a first thickness and having a first threshold voltage;

an NMOS transistor having a gate oxide film of the first thickness and having a second threshold voltage higher than the first threshold voltage;

a PMOS transistor having a gate oxide film of the first thickness and a third threshold voltage;

a PMOS transistor having a gate oxide film of the first

thickness and having a fourth threshold voltage whose absolute value is larger than the absolute value of the third threshold voltage;

an NMOS transistor having a gate oxide film of a second  
5 thickness thicker than the first thickness and having a fifth threshold voltage with the same impurity dose in a channel as that of an NMOS transistor having the second threshold voltage; and

a PMOS transistor having a gate oxide film of the second  
10 thickness and having a sixth threshold voltage with the same impurity dose in a channel as that of a PMOS transistor having the fourth threshold voltage,

the logic circuit comprises NMOS transistors of the first and second threshold voltages and PMOS transistors of the third  
15 and fourth threshold voltages; and

the input output circuit comprises an NMOS transistor having the fifth threshold voltage and a PMOS transistor having the sixth threshold voltage.

20 9. A semiconductor integrated circuit device according to claim 8, further comprising a memory cell array on which a number of memory cells are integrated, and

wherein the memory cell is a dynamic memory cell including one transfer MOS transistor and one capacitor, and the transfer  
25 MOS transistor in the memory cell is an NMOS transistor having

the fifth threshold voltage.

10. A semiconductor integrated circuit device according to claim 9, further comprising a memory cell array on which a number of memory cells are integrated, each of the memory cells is a dynamic memory cell having one transfer MOS transistor and one capacitor, and

the transfer MOS transistor in the memory cell is a transistor which has the same dose of an impurity in a channel as that of the NMOS transistor having the fifth threshold voltage and has a long channel.

11. A semiconductor integrated circuit device comprising:  
a logic circuit;

a level shifter circuit for converting a low voltage signal to a high voltage signal; and

a data input/output circuit,

wherein the circuits include:

an NMOS transistor having a gate oxide film of a first thickness and having a first threshold voltage;

an NMOS transistor having a gate oxide film of the first thickness and having a second threshold voltage higher than the first threshold voltage;

a PMOS transistor having a gate oxide film of the first thickness and having a third threshold voltage;

a PMOS transistor having a gate oxide film of the first thickness and having a fourth threshold voltage whose absolute value is larger than the absolute value of the third threshold voltage;

5        an NMOS transistor having a gate oxide film of a second thickness thicker than the first thickness and having a fifth threshold voltage with the same dose of an impurity in a channel as that of an NMOS transistor having the first threshold voltage;

10        an NMOS transistor which has a gate oxide film of a second thickness and has a sixth threshold voltage with the same dose of an impurity in a channel as that of the NMOS transistor having the second threshold voltage;

15        a PMOS transistor which has a gate oxide film of the second thickness and has the same dose of an impurity in a channel of the PMOS transistor having the third threshold voltage; and

a PMOS transistor which has a gate oxide film of the second thickness and has the same dose of an impurity in a channel of the PMOS transistor having the fourth threshold voltage,

20        the logic circuit includes the NMOS transistors of the first and second threshold voltages and the PMOS transistors of the third and fourth threshold voltages,

the input output circuit includes the NMOS transistor having the sixth threshold voltage and the PMOS transistor having the eighth threshold voltage; and

25        the MOS transistor for receiving the low voltage signal

in the level shifter circuit has the fifth threshold voltage of the gate oxide film of the second thickness.

12. A semiconductor integrated circuit device according to claim 11, further comprising a memory cell array on which a number of memory cells are integrated,

wherein the memory cell is a dynamic memory cell having one transfer MOS transistor and one capacitor, and

the transfer MOS transistor in the memory cell is an NMOS transistor having the sixth threshold voltage.

13. A semiconductor integrated circuit device according to claim 11, further comprising a memory cell array on which a number of memory cells are integrated,

wherein the memory cell is a dynamic memory cell having one transfer MOS transistor and one capacitor, and

the transfer MOS transistor in the memory cell is a transistor which has the same dose of an impurity in a channel as that of the NMOS transistor having the sixth threshold voltage and has a long channel.

14. A semiconductor integrated circuit device according to any one of claims 1 to 3,

wherein source and drain regions of the transistor are formed in a well of a first conductive type having a first

impurity concentration region and a second impurity concentration region,

the first impurity concentration region is in contact with a source electrode or a drain electrode and has impurity concentration higher than that of the second impurity region, and

the second impurity concentration region is in contact with a region having concentration higher than concentration of a second conductive type impurity of a second conductive type semiconductor substrate.

15. A semiconductor integrated circuit device according to claim 14, wherein the transfer MOS transistor has a gate length longer than that of the NMOS transistor having the first threshold voltage in the logic circuit, has the same dose of an impurity as that of the NMOS transistor, and has a gate voltage with which drain current becomes 1 nA per 1  $\mu\text{m}$ , which is equal to or higher than that of the drive MOS transistor.